

EX. WHEN NUT SETTING IS GIVEN TO CH 25  
 FROM NUT SETTING INFORMATION, NUT OF  
 CH25 IS ESTABLISHED AND NUT RELAY  
 INFORMATION IS RELAYED.

FIG. 1

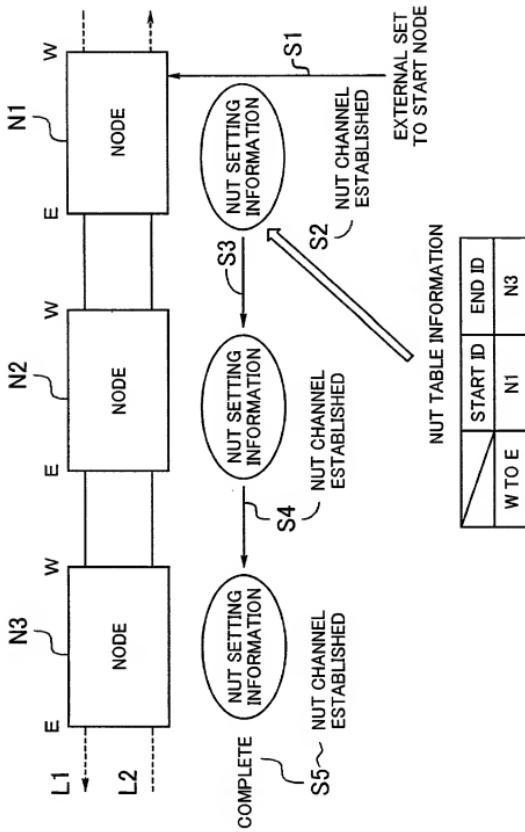


FIG. 2

2020EO-660600T

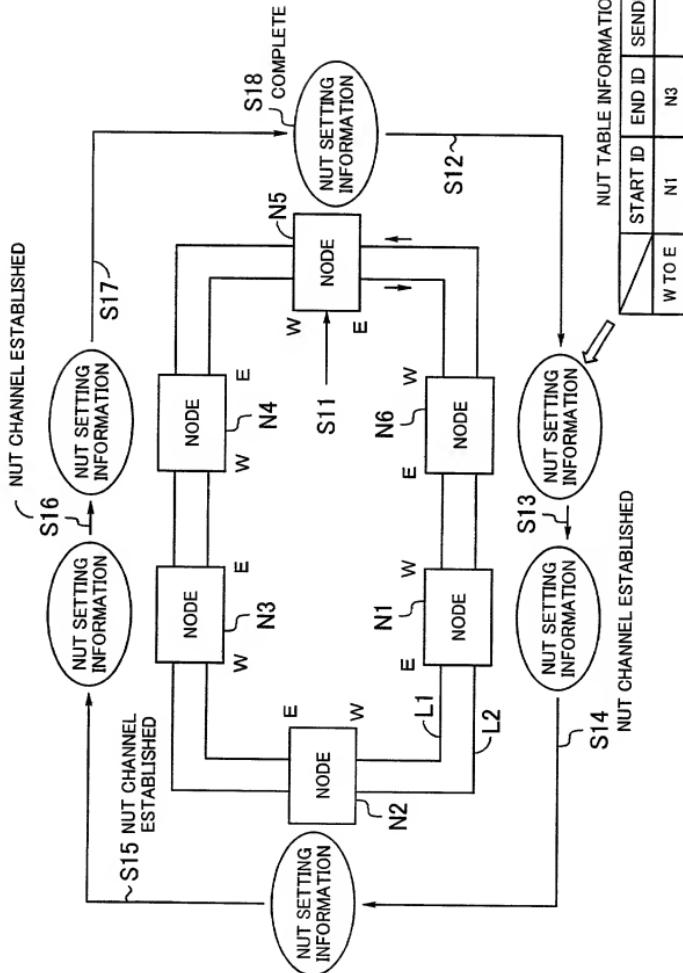


FIG. 3

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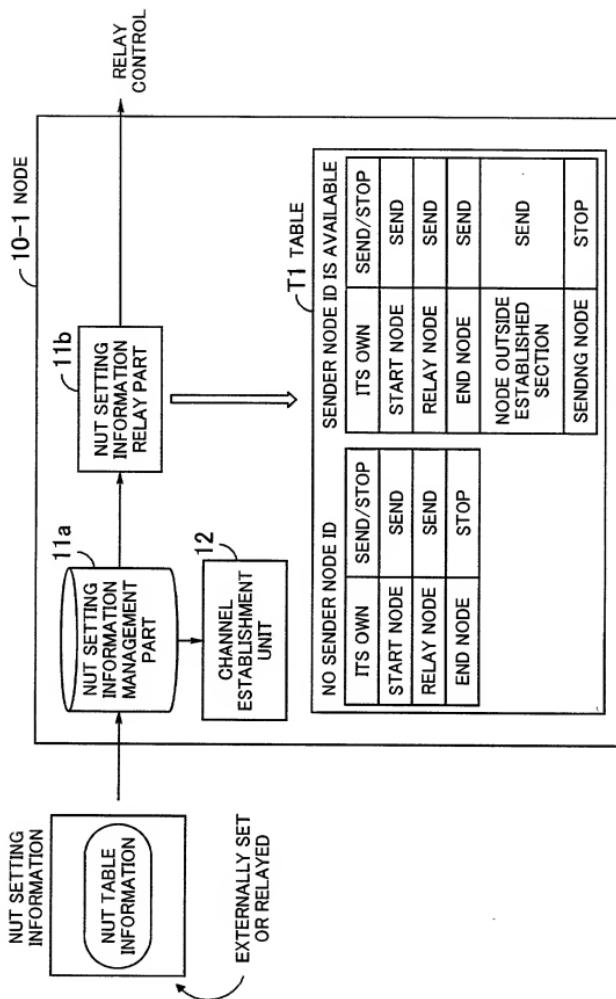
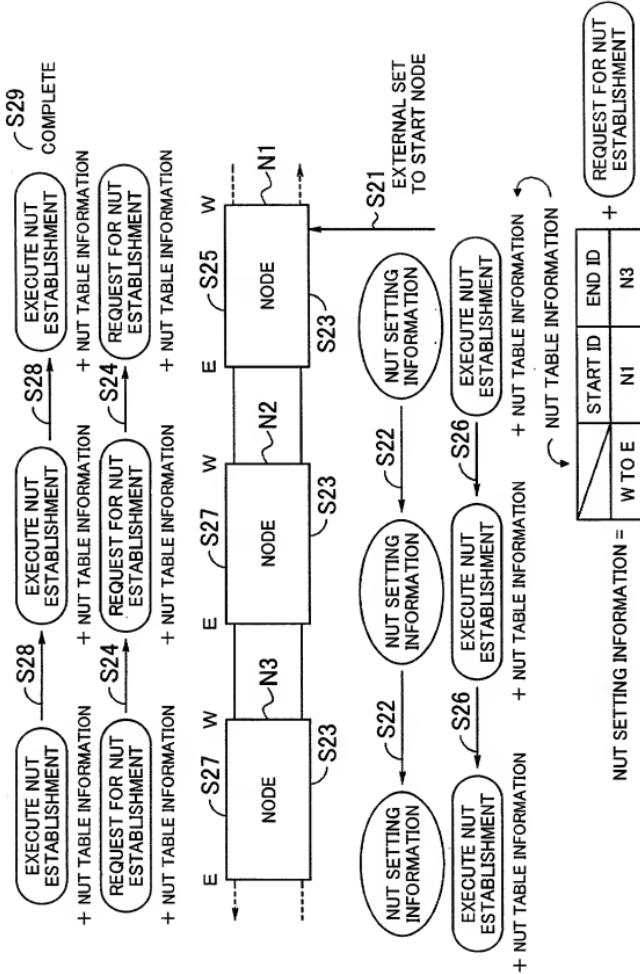


FIG. 4



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2050E0-6E606000F

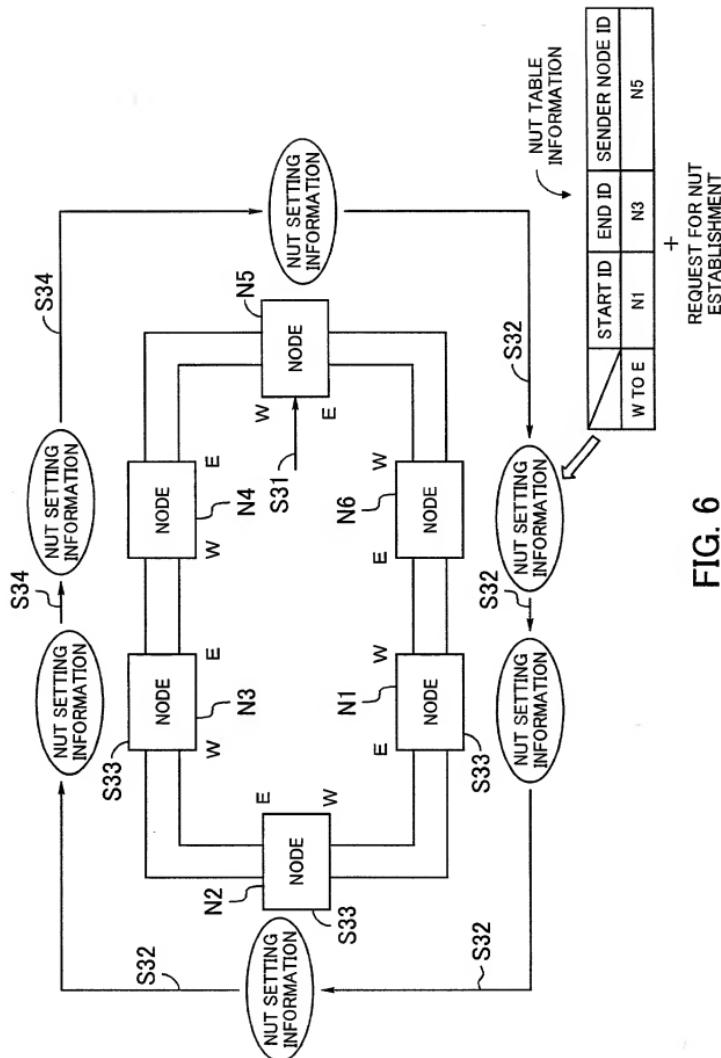
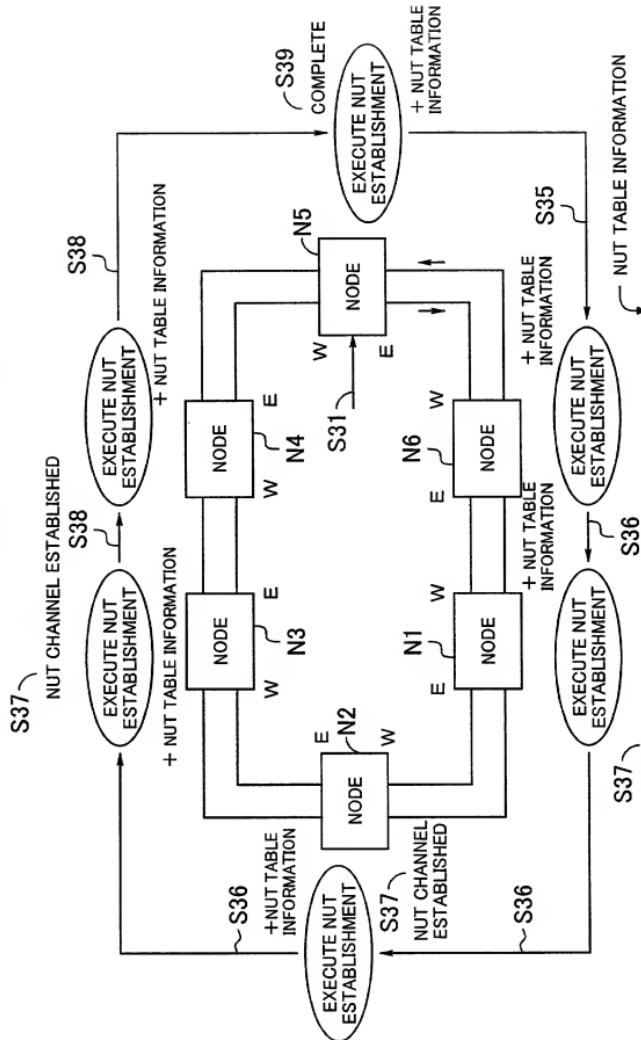


FIG. 6



7

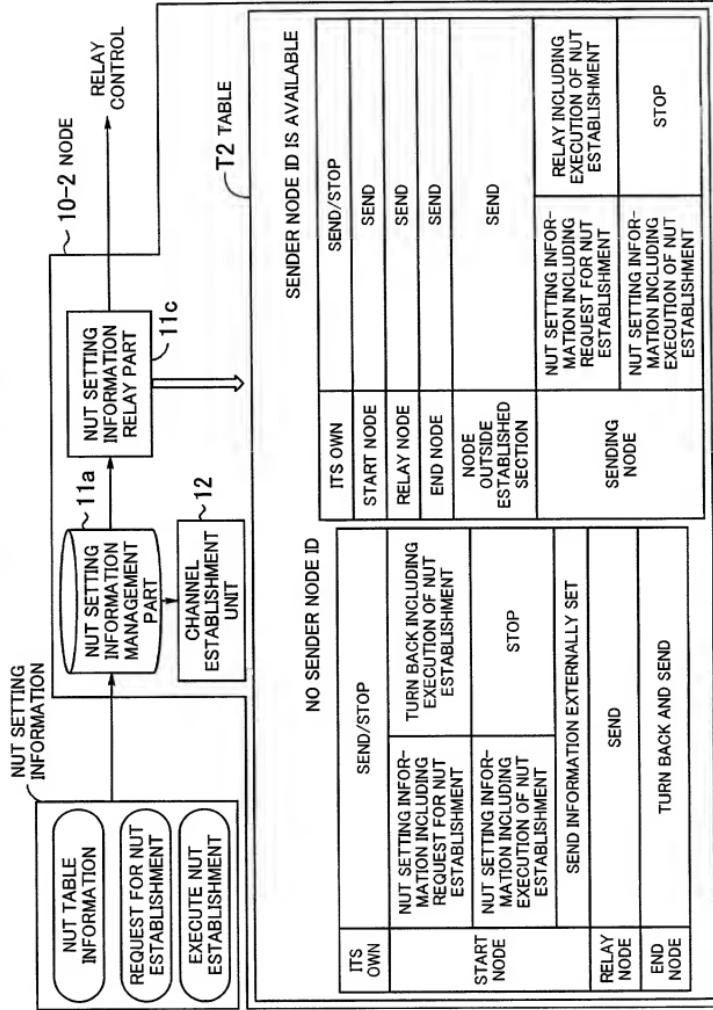


FIG. 8

BIT NUMBER		LSB							
		1	2	3	4	5	6	7	8
D6#2	DATA UPDATING BIT	MSB	1	PARITY	MSB	MSB	TABLE RAM ADDRESS(U)	MSB	LSB
D5#2	NUT/SQUELCH SHARING PART	MSB	MSB	MSB	MSB	MSB	TABLE RAM ADDRESS(L)	MSB	LSB
D5#3	NUT/SQUELCH SHARING PART	MSB	MSB	MSB	MSB	MSB	DST.NODE ID	MSB	LSB
D5#4	NUT/SQUELCH	1	MSB	MSB	MSB	MSB	CRC CHECK CODE	MSB	LSB
NEW NUT TYPE	EXCLUSIVELY USED BY NUT	NCHG	EW/WE	EW/WE	MSB	LSB	TABLE RAM ADDRESS	1	PARITY

FIG. 9

## 205160: ADDRESS

### D6#2 BYTE

#### BIT NO.

- 1: BIT INDICATING THAT DATA IS BEING UPDATED
- 2: FIXED TO "1"

- 3: ODD PARITY BIT FOR BITS 4-8

4-8: 5 UPPER BITS OF SQUELCH TABLE AND NUT TABLE RAM.

THESE BITS INDICATE ADDRESS OF NUT TABLE RAM TOGETHER WITH BITS 4-8 OF D6#2

### D5#2 BYTE

#### BIT NO.

1: PART EXCLUSIVELY USED BY SQUELCH TABLE

2: PART EXCLUSIVELY USED BY SQUELCH TABLE

3-8: SIX LOWER BIT OF ADDRESS OF SQUELCH TABLE AND NUT TABLE RAM.

THESE BITS INDICATE ADDRESS OF NUT TABLE RAM TOGETHER WITH BITS 4-8 OF D6#2

**FIG. 10**

DATA = 656565001

D5#3 BYTE

BIT NO.

1-4: SCR.NODE ID (START NODE ID)

5-8: DST.NODE ID (END NODE ID)

D5#4 BYTE

BIT NO.

1: BIT INDICATING TYPE OF INFORMATION TO BE TRANSFERRED

1: SQUELCH TABLE

0: NOT SETTING INFORMATION

2: FIXED TO "1"

3-8: CRC6 Check code (BITS SUBJECT TO CALCULATION: BITS 3-8 OF D5#2  
BITS 1-8 OF D5#3)

FIG. 11

2050E0 = 6E60600T

NEW BYTE

BIT NO.

1: BIT INDICATING TYPE OF NUT

1: BASIC NUT

0: ENHANCED NUT

2-3: BIT INDICATING NUT TABLE TRANSFER CONDITION

00: NUT SETTING RELEASE CONDITION

01: NUT SETTING RELEASE REQUEST CONDITION

10: NUT SETTING ESTABLISHMENT CONDITION

11: NUT SETTING ESTABLISHMENT REQUEST CONDITION

4: BIT INDICATING RELAY DIRECTION

1: EAST TO WEST (EW)

0: WEST TO EAST (WE)

5-6: GROUP IDENTIFIER. OC192 IS DIVIDED INTO FOUR GROUPS

7: FIXED TO "1"

8: ODD PARITY BIT FOR BITS 1-6

FIG. 12

GROUP	RAM	SPAN	CH-NO.	ADD/DROP
0	000	1	1	ADD
0	001	1	1	DROP
0	002	1	2	ADD
0	003	1	2	DROP
0	004	1	3	ADD
0	005	1	3	DROP
----	----	----	----	----
0	05E	1	48	ADD
0	05F	1	48	DROP
0	060	2	1	ADD
0	061	2	1	DROP
----	----	----	----	----
0	0BE	2	48	ADD
0	0BF	2	48	DROP
----	----	----	----	----
0	5A0	16	1	ADD
0	5A1	16	1	DROP
----	----	----	----	----
0	5FE	16	48	ADD
0	5FF	16	48	DROP

T3



FIG. 13

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GROUP	RAM	SPAN	CH-NO.	ADD/DROP
1	000	1	49	ADD
1	001	1	49	DROP
---	----	----	----	----
1	5FE	16	96	ADD
1	5FF	16	96	DROP
2	000	1	97	ADD
2	001	1	97	DROP
---	----	----	----	----
2	5FE	16	144	ADD
2	5FF	16	144	DROP
3	000	1	145	ADD
3	001	1	145	DROP
---	----	----	----	----
3	5FE	16	192	ADD
3	5FF	16	192	DROP

FIG. 14

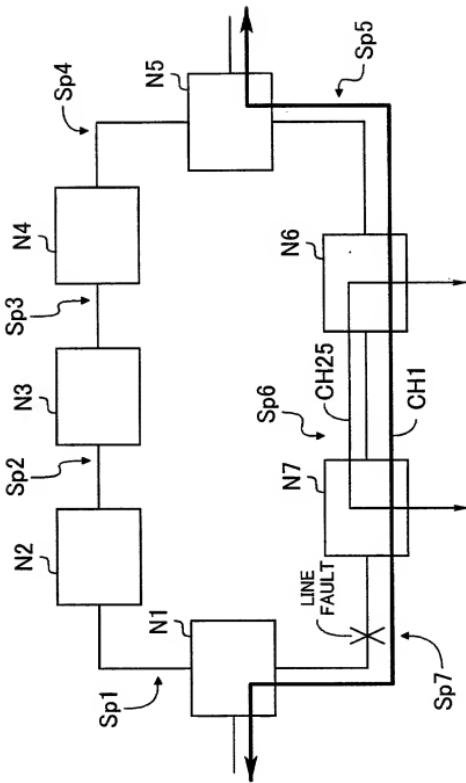


FIG.15

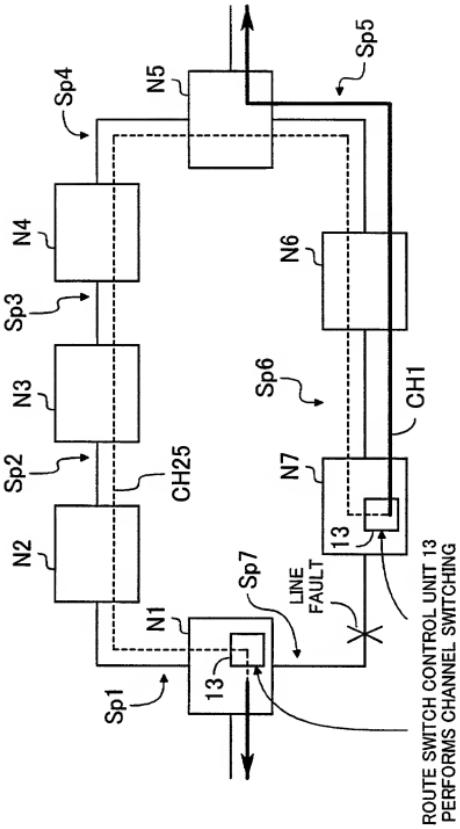
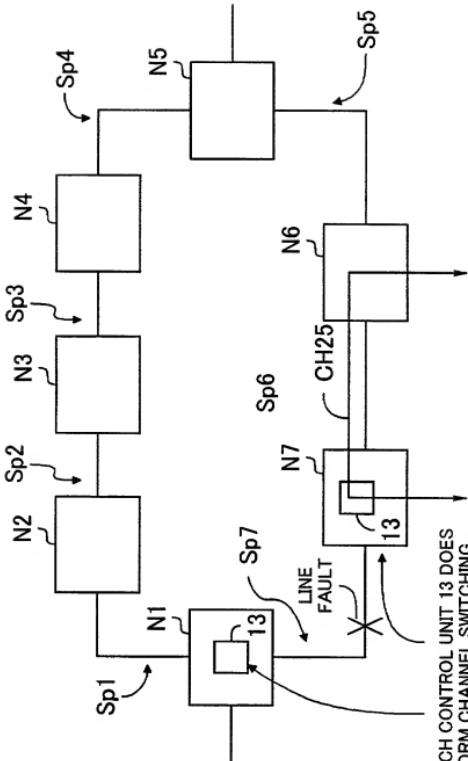


FIG. 16

ROUTE SWITCH CONTROL UNIT 13  
PERFORMS CHANNEL SWITCHING



ROUTE SWITCH CONTROL UNIT 13 DOES  
NOT PERFORM CHANNEL SWITCHING

FIG. 17

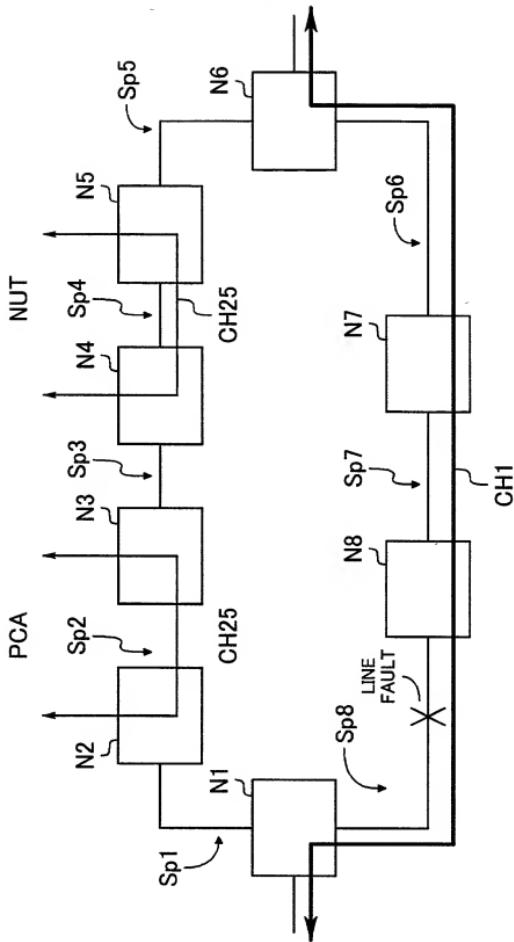


FIG. 18

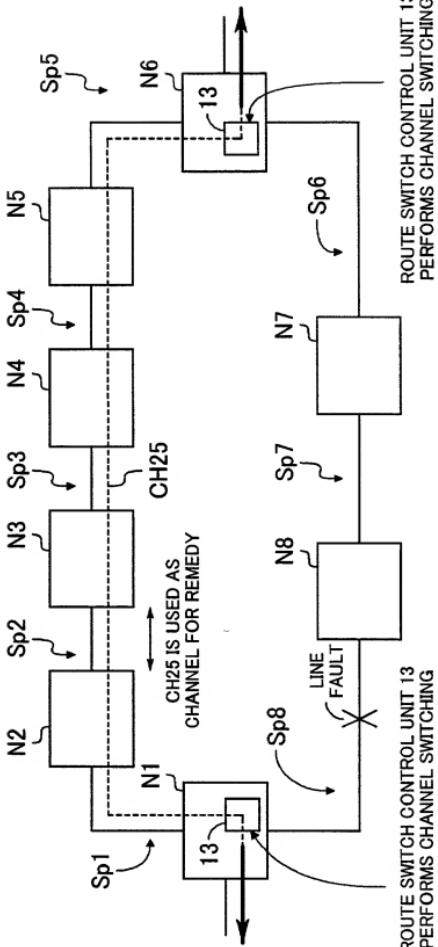


FIG. 19

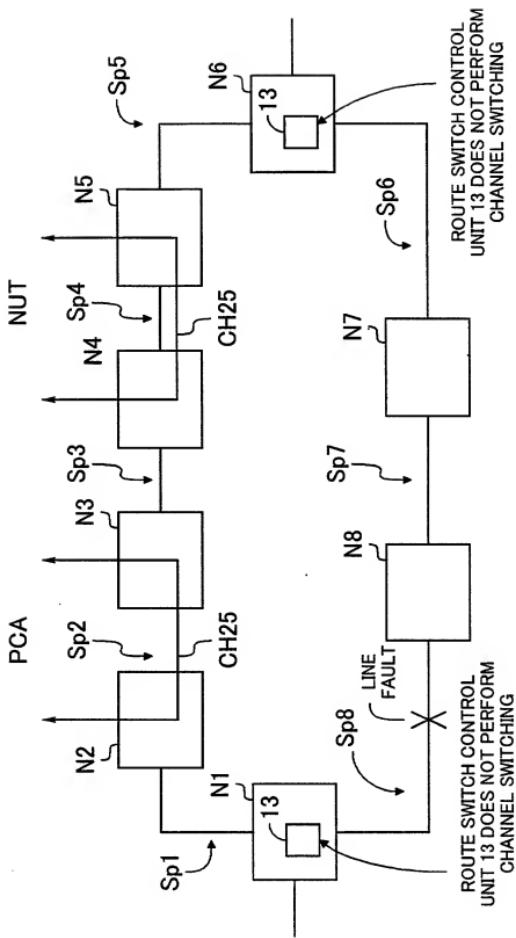
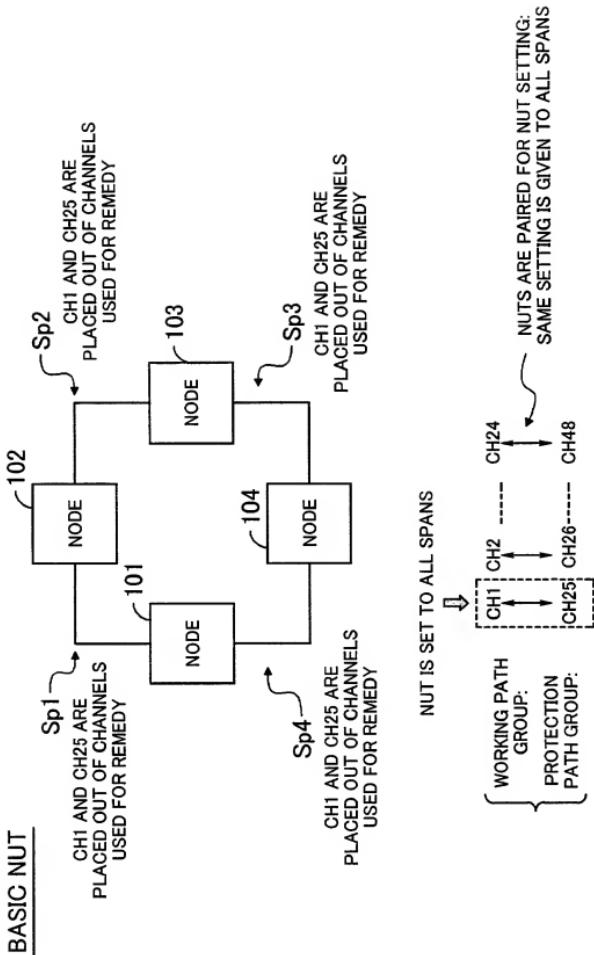


FIG. 20



**FIG. 21**  
**PRIOR ART**

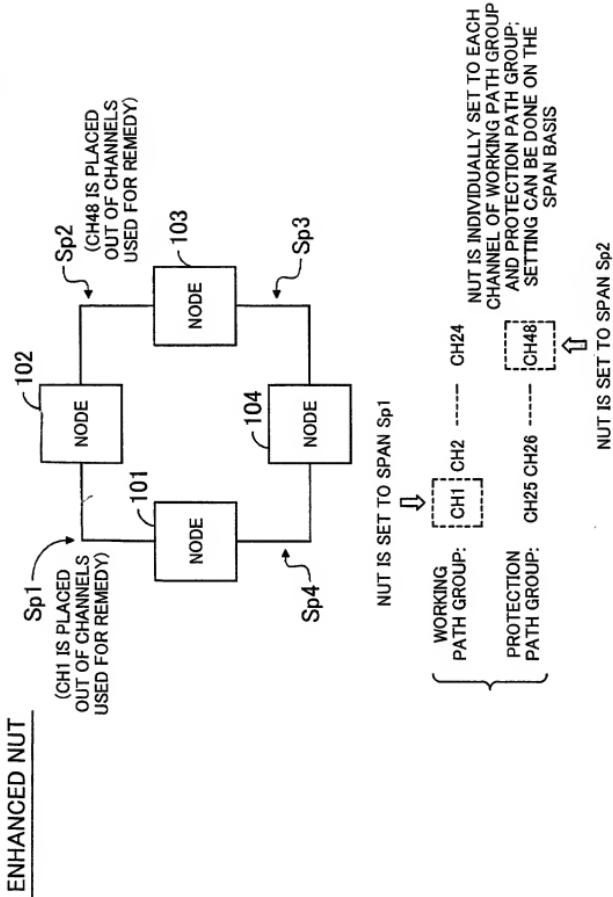


FIG. 22  
PRIOR ART